A 40Gb/s Adaptive Equalizer with Amplitude Approaching Technique in 65nm CMOS

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***Abstract*—An adaptive equalizer which operates at 40Gb/s using amplitude approaching technique is introduced in this paper. The proposed equalizer has a simple architecture to compensate the channel adaptively. The common mode detection of the equalizer filter output with the resister ladder that can generate the reference voltages depending on the common level of the output of the filter is presented as well. The simulation results show that the equalizer could compensate for 20dB channel loss at 20GHz. The jitter of equalized data is 2.8ps and the total power consumption is 40mW under the 1V supply voltage.**

Keywords—adaptive equalizer; amplitude approaching;

I. INTRODUCTION

As the data rate for high-speed communication systems increases rapidly, the limited channel bandwidth becomes a critical factor for processing serial data at tens of gigabits per second. In order to compensate for the severe degeneration of different channel at high frequency, various types of adaptive equalizers have been investigated for high-speed interface applications [1-3]. In the spectrum balanced method, typically, the low and high frequency component of signal power are compared to generate feedback signals which adjust the equalizers adaptively until the power spectrum is balanced [1]. However, the precision of this scheme is easily affected by data patterns for the fixed frequency that splits the spectrum into two parts with equal power. In addition, the capacitors in both filters and feedback loop occupy a large Si area [4]. The eye opening monitoring (EOM) scheme achieves the adaptive function by monitoring the eye diagram of date continuously [3]. Unfortunately, it is difficult to recover the clock from initial closed eye diagram. Digital signal processing technique based on maximum likelihood sequence detection is also a good method for adaptive equalization, but it has disadvantages in speed limitation and complicated architecture of ADC [2]. Another excellent scheme can be used for adaptive equalization is based on the simple observation that the clearest eye diagram produces the largest peak value when data histograms are taken [4]. For this method, it takes regular scanning time to select the optimal equalizing filter code for a given channel which always consumes some extra power. Some other techniques applied in the adaptive equalization only perform very well in low date rate, and can also be easily affected by the variation of the process, voltage, temperature (PVT) [5].

In this paper, we present a 40Gb/s adaptive equalizer with a novel scheme. The critical idea to implement this scheme is the assumption that the amplitude of both the data's DC and high frequencies component is nearly the same when the equalizer achieves the best optimization. The core circuit of the adaptive equalizer is a digital controller which is synthesized by Hardware Description Language (HDL). Therefore, the equalizer consumes lower power and occupies a smaller area. Besides, our adaptive equalizer converges in a pretty short time and has superior robustness under PVT variation.

This paper is organized as follows: Section II presents the proposed adaptive equalizer architecture and building blocks. The adaptive equalization mechanism is introduced in Section III. The simulation results are shown in Section IV. Conclusions are presented in section V.

II. ARCHITECURE

Fig.1 presents the overall design of the proposed adaptive equalizer. The equalizer consists of a continuous time linear equalizer (CTLE) path which boosts the data received from channel and an adaptation loop which finds the optimum eye opening point.

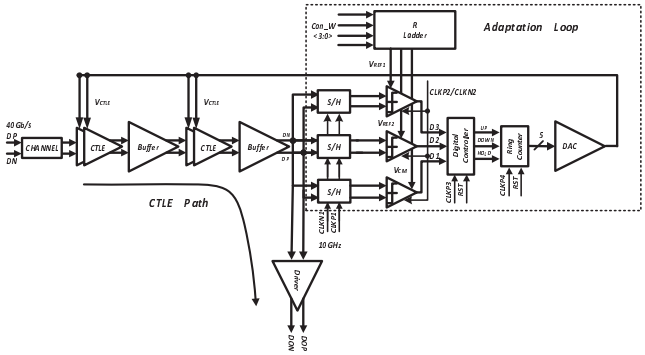


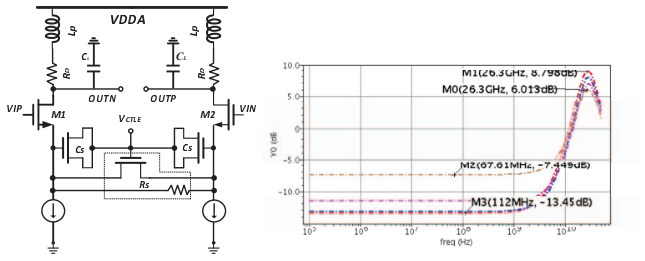
Fig.1. Block diagram of the proposed adaptive equalizer

The sample-hold circuit (*S/H*) works at 5GHz and the sampled data will be compared with three reference voltages V_{CM}, V_{REF1}, V_{REF2} simultaneously. These reference voltages are criteria of the equalizer output conditions. The *Digital Controller (DG)* records the pulse numbers of D1, D2 and D3 produced by three dynamic three-input comparators to generate control signals for 5-bit *Ring Counter* (*RC*) every other 256 clock cycles. The *RC* begins to count according to the control signals UP, DOWN and HOLD, and then delivers the 5-bit signal to the *Digital-to-analog Converter (DAC)*. The *DAC* converts the 5-bit signal to analog voltage (*VCTLE*) to

adjust the gain boost of the CTLE. The *Resister Ladder* (*R Ladder*) produces reference voltage for eye measuring. A *4-bit Control Word (Con_W)* is utilized to select the reference voltages of the *R Ladder*. The current model logic (*CML*) buffers are used to compensate for DC loss. The boosted data from the equalizer come out through the *CML* type output driver for the test purpose.

A. Equlizer Filter and R Ladder

In order to equalize 40Gb/s data, the CTLE must provide wide bandwidth and remarkable capability of large boosting at high frequencies. Traditional approach incorporating capacitive degeneration technique to generate tunable boosting can't satisfy the requirements. To further extend the bandwidth and enlarge the boost, each filter stage is realized with capacitive degeneration and inductive peeking, as shown in Fig.2-(a). The conclusion in [1] shows that this topology facilitates the equalizer filter's design and makes the 15-20 dB compensation at 20GHz become feasible. Fig.2-(b) shows the AC response of the cascaded filters when *VCTLE* changes from 0.6V to 0.9V with 100mV step. Simulation shows that the cascaded filters stage can make about 13.4dB-22.4dB compensation.

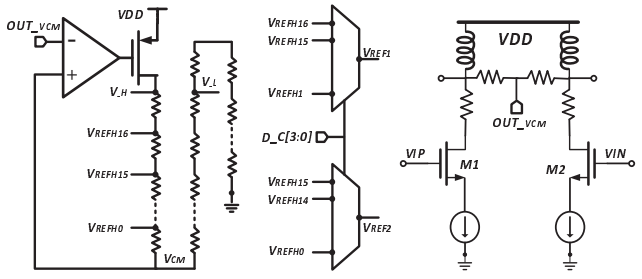


(a) (b)

Fig.2. Proposed equalizing filter: (a) the architecture of filter, (b) the AC response of filter in different *VCTLE*

B. R Ladder and CML Buffer

The schematic of the R ladder [5] is shown in Fig.3-(a). Forty resisters are connected serially. There are 18 resisters on each side of the V_{CM} node. These resisters slice the voltage to 36 levels, and V_{CM} is the center of these voltages. A PMOS with a single ended amplifier is connected to the top of the resisters to track the output common mode voltage of the buffer (OUT_{VCM}) with V_{CM}.



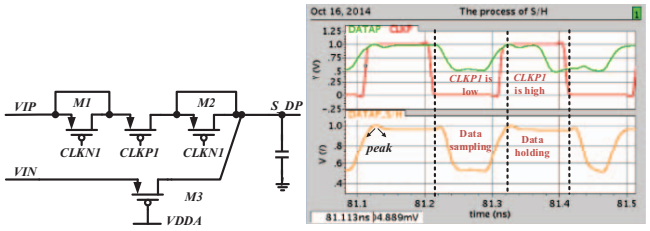
(a) (b)

Fig.3 (a) the architecture of R ladder, (b) the proposed CML buffer

To extend the bandwidth even further, we choose the CML buffer with inductive peeking, as shown in Fig.3-(b). Two cascaded CML buffers result in a total gain of 6dB, which could be used to compensate for DC loss.

C. S/H Circuit

The pass-gate S/H circuit are fully differential, but for simplicity a half circuit schematic is shown in Fig.4-(a). In addition to the primary pass-gate device, dummy switches (M1 and M2) cancel the clock feedthrough, while M3 cancels the differential data feedthrough during the hold phase [6].



(a) (b)

Fig.4. (a) half circuit of S/H, (b) S/H operates in sample and hold phase

For the speed limitation of the three-input comparator, S/H works suitably at 5GHz. Under the right conditions, S/H should sample the data at the center of the eye diagram and hold for some time until the three-input comparator completes comparison. Fig.4-(b) shows the results when S/H operates in sample and hold phase, respectively. In Fig.4-(b), *S_DP* follows the *DATAP* when *CLKP1* is low and keeps the value at the center of data when *CLKP1* is high, which suggests that S/H circuit works in right conditions. The small peak appearing ahead of the hold phase is caused by the rising edge of the *CLKP1*. By adjusting the phase of *CLKP2* subtly, this small peak almost doesn't produce influence on the comparison result.

D. Dynamic Three-input Comparator

The dynamic three-input comparator consists of two slicers, four inverters, one OR gate whose architecture is shown in Fig.4. The slicer shown in Fig.4 is a double-tail latch-type voltage sense amplifier (SA) [7] which uses one tail for the input stage and another for the latching stage. The double tail enables both a large current in the latching stage (wide M12) for fast latching independent of the common-mode voltage of the input (*Vcm*), and a small current in the input stage (small M9)for low offset.

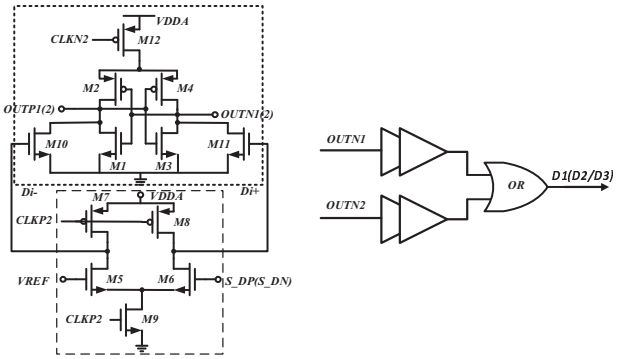


Fig.4 The proposed three-input comparator

Another significant advantage of the slicer is the low threshold voltage. Even if the difference between two inputs is about 6 mV, the slicer can also make decision correctly. The inputs of the slicer are the sampling differential voltage *S_DP* and *S_DN* at the center of data. Fig.5 shows the behavior of the double-tail SA when the difference between *S_DP* and *S_DN* varies from 300mV to 6mV.

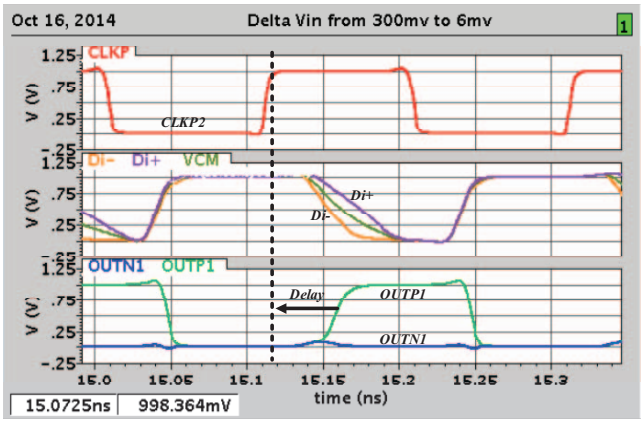


Fig.5 The behavior of the double-tail SA

In order to detect the sampled date's voltage, each sampled data should be compared with the reference voltage, then the comparisons between S_DP and VREF, S_DN and VREF will pass through OR gate to generate the D pulse.

E. DG and RC

As mentioned before, both DG and RC are synthesized by HDL, therefore they consume lower power and occupy a smaller area. The function of DG is to record the pulse numbers of D1, D2 and D3 produced by three dynamic three-input comparators. For every other 256 clock cycles, the DG compares the pulse numbers of D1 with that of (D2+D3) and then generates the control signals UP, DOWN and HOLD accordingly. The relationship between control signals and comparison results is shown in table I.

Table I THE RELATIONSHIP BETWEEN CONTROL SINGNALS AND THE COMPARISON RESULTS

Control signals	UP	DOWN	HOLD
D1>(D2+D3)	1	0	0
D1=(D2+D3)	0	0	1
D1<(D2+D3)	0	1	0

The *RC* begins to count according to the control signals UP, DOWN and HOLD. At the rising edge of CLKP4, the RC will increase (decrease) one when detecting a high level on UP(DOWN),and make no change when detecting a high level on HOLD. Finally the 5-bit counting signals are delivered to *DAC*.

III. ADAPTIVE EQUALIZATION MECHANISM

As the CTLE provides frequency peaking at the cost of attenuating low frequency component, there is an optimum state where both the high frequency component and the low frequency component of the equalized data have the same peak level. The goal of the adaptive loop is just to find the optimal reference voltage V_{REF1}, V_{REF2} which could cover the most peak level of data. In the initial state, the 4-bit *Con_W*[3:0] are set to all zero and therefore, the initial reference voltages V_{REF1}, V_{REF2} are set to their maximum value. When the equalizer begins to boost the received data, the comparator connected with voltage V_{CM} detects the center crossing of the boosted data, and generates the D1 pulses. The comparators connected with two voltages V_{REF1} and V_{REF2} produced by the *R ladder* detect the peak level of the boosted data and generate the D2 and D3 pulses. In each cycle, when the number of D1 pulses reaches to 256, the DG makes comparison between the pulse numbers of D1 and (D2+D3) and then generates the control signals for RC. The *RC* begins to count according to the control signals UP, DOWN and HOLD. Meanwhile, the *DAC* converts the 5-bit counting signal to analog voltage (*VCTLE*) to adjust the gain boost of the CTLE. In order to ensure the *VCTLE* converge to a stable voltage, we could configure the *Con_W*[3:0] from [0000] to [1111] manually. When the *Con_W*[3:0] comes to its appropriate value, the suitable reference voltage V_{REF1}, V_{REF2} which could cover the most peak level of data are obtained, which means the *VCTLE* converges to a stable voltage.

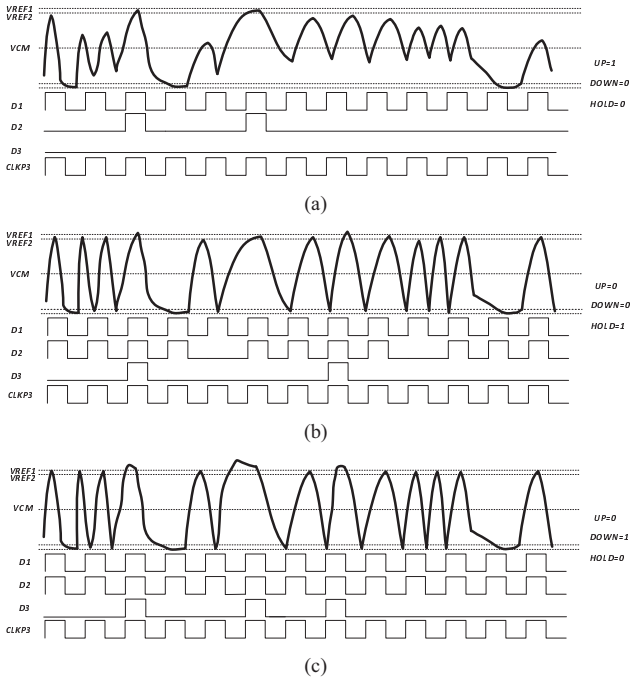


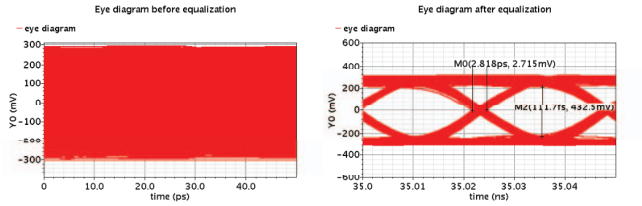
Fig.6 Three states for adaptive equalization: (a) under-equalization, (b) optimum equalization, (c) over-equalization

Fig.6 indicates three states of the adaptive loop under the ***optimal reference voltage*** V_{REF1}, V_{REF2}. When the equalizer starts to boost, the eye of the CTLE output is under-equalized as shown in Fig.6-(a). In this state, the number of D1 pulses is much larger than the sum of D2 and D3 pulses. Therefore, the control signal UP is enabled and the V_{CTLE} is increased by the CP. As V_{CTLE} keeps increasing, the number of D2 pulses increases, and a few D3 pulses show up due to the low

frequency bits of data. The V_{CTLE} stops increasing when the number of D1 and the sum of D2 and D2 pulses are the same as shown in Fig.6-(b). When the eye is over-equalized, as shown in Fig.6-(c), the number of D1 pulses is less than the sum of D2 and D3 pulses, therefore the DOWN is enabled and the V_{CTLE} is suppressed. By this adaptive mechanism, we could easily find the optimal pair of reference voltage V_{REF1}, V_{REF2} to cover the most peak level of data.

IV. Simulation Results

The presented adaptive equalizer is designed in 65nm CMOS technology. To verify this design, a lot of simulation has been done under various environment. The channel is a model of RLGC and has a 20dB loss at 20GHz. Fig.7 shows the equalized eye diagram of 40Gb/s in PRBS-31 data pattern when driving the 150fF capacitor and 50 ohm resistor in SS corner, 85℃. The jitter is only 2.8ps and the height of eye diagram is 432.5mV.



(a) (b)

Fig.7. Eye diagram when driving the 150fF capacitor and 50 ohm resistor: (a) before equalization, (b) after equalization

Under the optimal reference voltage V_{REF1}, V_{REF2}, the adaptive curve of VCTLE is shown in Fig.8. As the Fig.8 depicts, the final VCTLE voltage fluctuates around 840mV and the convergence time is about 690ns.

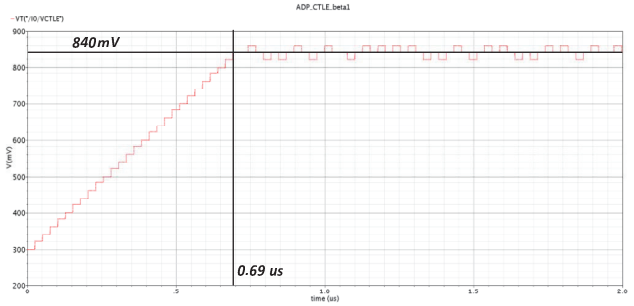


Fig.8 The adaptive curve of VCTLE

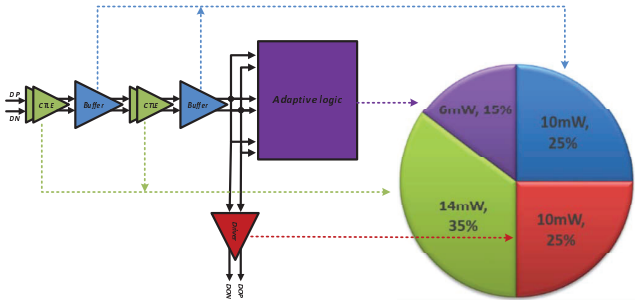


Fig.9 The adaptive equalizer core's power distribution

The total simulation power consumed by the adaptive equalizer core is 40mW, as shown in Fig.9. The compared results with other works are listed in the Table.II.

Table II Comparison to Other Works' Designs

Reference	[1]	[2]	**This work***
Data Rate(Gb/s)	20	5.4	**40**
Process Technology	130nm	130nm	**65nm**
Technique	Spectrum balance	Unit pulse charging	**Amplitude approaching**
Energy/bit(PJ/b)	3	3.23	**1**
Power Dissipation(mW)	60	17.64	**40**

*Don't include the power of clock distribution network

I. Conclusion

An adaptive equalizer which operates at 40Gb/s with amplitude approaching technique is introduced in this paper. The equalizer consists of a continuous time linear equalizer path which boosts the data received from channel and an adaptation loop which finds the optimum eye opening point. The proposed method has a simpler architecture and lower power consumption than other works. The simulation shows that the eye opening is 432.5mV with 2.8ps jitter and the total power consumption is 40mW.

Acknowledgment

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References

[1] J. Lee, "A 20-Gb/s adaptive equalizer in 0.13-µm CMOS technology," IEEE J.Solid-State Circuits, vol. 41, no. 9, pp. 2058–2066, Sep. 2006.

[2] O.E. Agazzi, et al, "A 90nm CMOS DSP MLSD transceiver with integrated AFE for electronic dispersion compensation of multimode optical fibers at 10 Gb/s," IEEE J. Solid-State Circuits, vol.43, no. 12, pp. 2939-2957, Dec. 2008.

[3] B. Analui, A. Rylyakov, S. Rylov, M. Meghelli and A. Hajimiri, "A 10-Gb/s twodimensional eye-opening monitor in 0.13-µm standard CMOS," IEEE J. Solid-State Circuits, vol. 40, pp. 2689–2699, Dec. 2005.

[4] W.-S. Kim, C.-K. Seong, and W.-Y. Choi, "A 5.4-Gb/s adaptive equalizer using asynchronous-sampling histograms," in *Proc. IEEE ISSCC Dig.Tech. Papers*, Feb. 2011, pp. 358–359.

[5] Sewook Hwang, Inhwa Jung, Junyoung Song, Chulwoo Kim, "A 5.4Gb/s Adaptive Equalizer with Unit Pulse Charging Technique in 0.13µm CMOS," Proceedings of 2012 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1959 –1962, June 2012.

[6] Ankur Agrawal, John F. Bulzacchelli, Timothy O. Dickson,Yong Liu, JoseA. Tierno and Daniel J. Friedman, "A 19-Gb/s Serial Link ReceiverWith Both 4-Tap FFE and 5-Tap DFE Functions in 45-nm SOI CMOS," IEEE J.Solid-State Circuits, vol. 47, no. 12, pp. 3220-3231, Dec. 2012.

[7] Daniel Schinkel, Eisse Mensink, Eric Klumperink, Ed van Tuijl, Bram Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," in *Proc. IEEE ISSCC ANALOG.Tech. AND PLLs Papers*, Feb. 2007, pp. 314–315.