A 40Gb/s 27mW 3-tap Closed-loop Decision Feedback Equalizer in 65nm CMOS

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***Abstract*—This paper describes design techniques of enabling energy-efficient 3-tap decision feedback equalizer (DFE) to operate at 40Gb/s in 65nm CMOS technology. First, we propose a closed-loop architecture utilizing three techniques to achieve the 1st tap stage design, namely a merged latch and summer, reduced latch gain, and a dynamic latch design. Then, we suggest to merge the feedback MUX with the tap differential pairs within clock-control summers array (CCSA) to accomplish the 2nd and 3rd tap stages design. The total power consumption of the 3-tap DFE is 27mW under 1V, achieving 0.67 pJ/bit energy efficiency.**

Keywords— 3-tap DFE; closed-loop; dynamic latch; clock-control summers array; energy efficiency;

I. INTRODUCTION

With the high-speed wireline data communication such as chip to chip serial links in excess of 40-Gb/s, the limited channel bandwidth definitely causes severe post-cursor inter-symbol interference (ISI). Besides, the power consumption of broadband communication becomes significantly critical in multi-lane applications such as the 100 Gigabit Ethernet. However, the power-speed trade-off tends to intensify at higher rates, making it a greater challenge to reach the generally-accepted efficiency of 1mW/Gb/s [1]. Given this trend, equalizer circuits—and particularly power efficient DFE designs—are constantly being pushed to operate at ever-higher speeds [2]. The feedback nature of a DFE is to achieve timing closure of the feedback loop that enables previous bit decision to effectively influence the current bit decision, and that are hence increasingly challenging to meet with data-rates increasing.

In order to relax the critical timing constraint of the initial tap(s), many current 20–40Gb/s designs utilize a loop-unrolled/speculative architecture[3][4]. However, speculative architecture introduces additional delay into the critical paths of later (non-unrolled) DFE taps due to the selection MUXes, and with its exponential growth in complexity, does not scale well as the number of unrolled taps increases. Perhaps for this reason, only one multi-tap DFE solution in [2] has been demonstrated at data rate > 40Gb/s.

In this paper, we utilize the techniques in [2] to directly close the most timing-critical 1st tap. Furthermore, we propose another technique to close the 2nd and 3rd taps, which is promising for saving power consumption significantly. Utilizing these techniques, we will present a 3-tap power efficient closed-loop DFE in 65 nm CMOS technology which works at up to 40Gb/s while consuming only 27mW under a 1V supply.

This paper is organized as follow: Section II presents the proposed 3-tap DFE architecture and the main techniques to close three taps and save power consumption. The simulation results are shown in Section III. Conclusions are presented in section IV.

II. PROPOSED CLOSED-LOOP DFE ARCHITECTURE

The block diagram of the proposed 3-tap closed-loop DFE is presented in Fig.1. Both the 2nd and 3rd tap work at quarter rate while the 1st tap operates on full rate. In order to relax the critical timing constraint in the 1st tap stage, we use latched summers (***Gm2***) to close the 1st tap. Note that this design technique can't achieve high gain, therefore we add a gain stage (***Gm1***) in front of the latched summer to compensate the gain remove from it. For the sake of avoiding serialization within the digital feedback path, two separate CCSA are placed before the 1st tap latched summer to cancel the 2nd and 3rd tap ISI. These linear summation nodes are also convenient locations to independently cancel the overall offset voltage on each path. Now that all of summer stages are realized by clock-control technique, the power dissipation will decrease significantly.

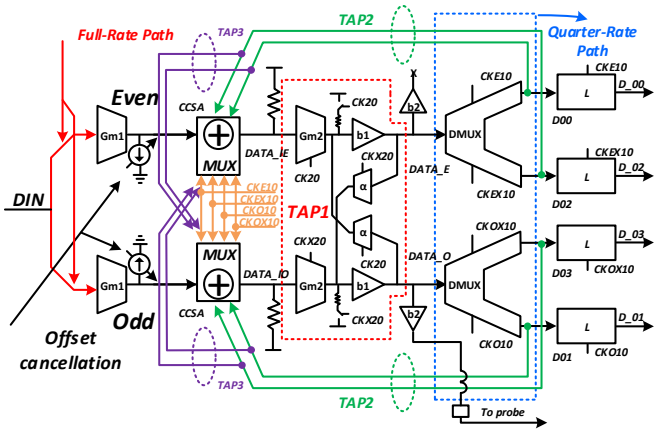

Fig.1. The proposed 3-tap DFE

In order to enable external measurements of the eye-

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diagram after equalization, a probe buffer (b2) is added at the output of the 1st tap latched summer. However, this additional capacitive loading along with the capacitive loading from the feedback pair, DMUX, and wiring result in a relatively high fanout(~4) for the latched summer, which would compromise the overall delay and efficiency. Therefore, a buffer (b1) is inserted at the output of the latched summer to help reduce the latched summer fanout to 1.5 and so that its speed is improved.

A. 1st Tap Stage Implementation

To relax the stringent 1st tap timing constraint, we adopt the optimization design techniques in [2]. First, as Fig.2-(b) shows, we merge the forward and backward summer stages with larches so that the latency of the feedback loop (green line) can be reduced to a single latch delay $T_{dq} < 1UI$, while in traditional architecture (Fig.2-(a)), the timing constraint of critical path (red line) is $T_{ckq}+T_{settle}+T_{setup} < 1UI$. Because T_{dq} is roughly equal to the T_{setup}, the timing constraint in Fig.2-(b) will be improved greatly. However, even a single T_{dq} in traditional latch may exceed the target bit time. Most RX designs place a large gain (often >10) in the latch in order to ensure that the output of the latch is "digital", nonetheless, this gain comes at the cost of larger T_{dq}.

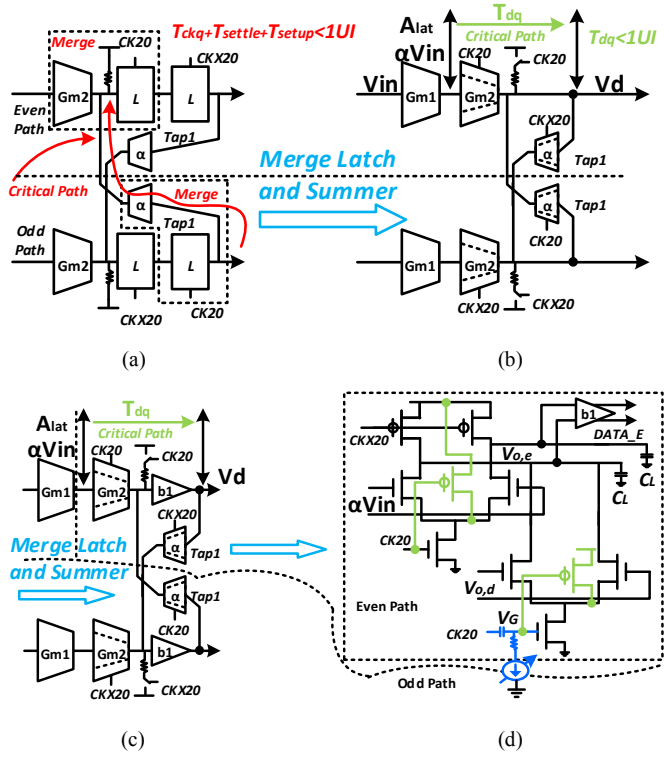


Fig.2. The implementation of the 1st tap stage: (a) the traditional 1st tap stage design, (b) the proposed 1st tap stage design, (c) the entire 1st tap stage design (d) the 1st tap stage implemented with dynamic latch

Fortunately, the gain of the latch in the DFE can be substantially reduced without impacting the function of DFE. Actually, as long as the output amplitude of the latch can drive the input pair of DFE feedback tap into its non-linear (clipped) region, the DFE operates as intended. In other words, if the feedback-tap pair's over-drive voltage (***V****) is sufficiently small relative to the input signal, the gain of the latch and hence its delay can be reduced to minimal levels. Note that the original input signals are usually small, we add a gain stage (***Gm1***) in front of the latch summer to compensate the gain removed from it, as long as the DFE's input stage is sufficiently linear.

Finally, we leverage the fact that the latch need not achieve high gain and implement it using a dynamic design in [5], just as Fig.2-(d) shows. To minimize the latch's sampling aperture, a PMOS tail reset device is added to actively turn off the latch input pair. Although NMOS transistor's f_T is superior to PMOS's, pre-charging the tail node all the way to Vdd with PMOS would substantially speed up the turn-off time. Note that adding PMOS pre-charge devices still delay the turn-on transition by 2–2.3 ps. However, since both the forward and feedback latch have such devices, the critical ***1UI*** timing won't be compromised by this extra delay. Combining these ideas enables the 1-tap DFE to operate at 40Gb/s successfully.

As mentioned before, a buffer (b1) is inserted at the output of the dynamic latch to help reduce the dynamic latch's fanout and the entire 1st tap stage design is shown in Fig.2-(c). In this 1-tap stage design, we use a small ***V**** (~175mV) for the ***Tap1*** pair. Hence, a higher ***V**** (~300mV) is used for the ***Gm2*** pair to allow larger input swing. This specific ***V**** is chosen to avoid significant penalty in current efficiency, resulting in a latch gain of ~1.5.

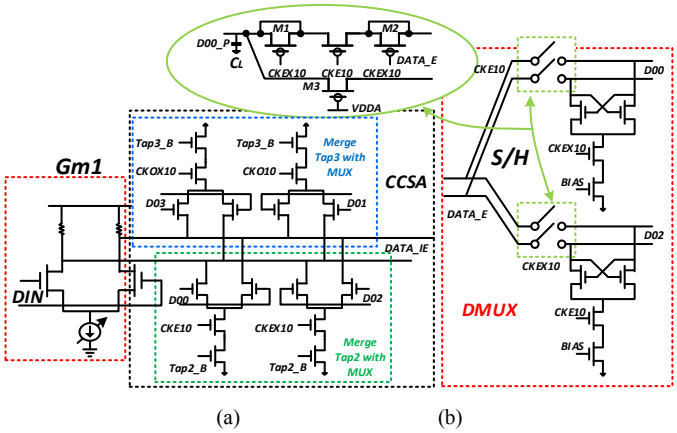
Although the overall gain target for our design is ~3.8, we chose a gain of only ~1.5 for the gain stage since it is loaded by the 2nd and 3rd feedback taps as well as the offset cancellation. The latched summer and buffer gains are set to ~1.5 and ~1.7 to achieve the optimal loop delay.

B. 2nd and 3rd Tap Stages Design

Now that we are able to close the most timing-critical 1st tap stage without introducing extra delay to later taps, it is relatively easy to close the 2nd and 3rd tap stages. As the Fig.3-(a) shows, in order to avoid the need for serialization within the digital feedback path, the 2nd and 3rd tap of the DFE are realized by two separate CCSA placed before the 1st tap latch summer. The architecture in the Fig.3 merits three remarks. First, the DMUX employs passive switching (S/H) but also boosts the sampled signal level by 6dB through the use of a regenerative positive feedback pair. Second, the S/H circuit should be designed elaborately to avoid bringing in extra ISI to 2nd and 3rd feedback stages. Third, this architecture merges the feedback MUX with the tap differential pairs within the summers, relaxing the loop timing obviously and achieving low power consummation significantly.

The amplitude of the equalized signals is usually small when channel loss is up to 20dB, therefore the kickback noise of S/H circuit may affect the DMUX's output easily and impact the function of the 2nd and 3rd feedback stages finally. This is the reason why we emphasize the careful design of S/H

circuit. The pass-gate S/H circuit [6] are fully differential, but for simplicity a half circuit schematic is shown in Fig.3-(b). In addition to the primary pass-gate device, dummy switches (M1 and M2) cancel clock feedthrough, while M3 cancels the differential data feedthrough during the hold phase .



(a) (b)

Fig.3. The design of the 2nd and 3rd tap stages: (a) the merged feedback MUX with tap differential pair in CCSA, (b) DMUX employs passive switching and positive feedback pair

C. Clock Distribution Network

In order to simplify testing, on-chip clock generator is not included in this initial prototype DFE design. However, the differential clocks provided to latch summer is necessary. The clock network of the 1st tap stage is similar to [2]. First, an on-chip balun is used to convert an external single-ended clock into the differential clocks needed by latch summer operation. We use DAC+AC coupling capacitors to provide the bias voltage for PMOS load and NMOS tail devices of dynamic latches. All of the other bias voltages, including the 2nd and 3rd tap coefficients are also provided by DAC. The clocks provided to the 2nd and 3rd stages are generated by on chip divider. All versions of the clock signals retain 1 V of single-ended peak-to-peak swing and the whole clock distribution network is shown in the Fig.4.

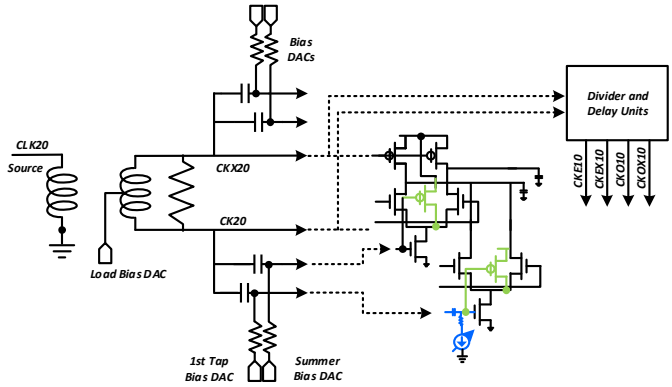


Fig.4. The clock distribution network

In order to understand the equalization process of the proposed 3-tap clearly, we utilize the timing diagram in Fig.5 to demonstrate how the DFE operates at 40Gb/s data rate. For each bit data, it has 1UI time in summation (transparent) phase and 1UI time in latch (opaque) phase, which are marked with letter ***S*** and ***L*** in ***DATA_E/DATA_O*** line of Fig.5, respectively. Taking ***D03*** for an instance, when ***CKX20=1***, both the PMOS triode loads and NMOS tail current source are enable so that the latched summer in ***Odd*** path is in its ***S*** phase. Meanwhile, the latch summer in the ***Even*** path has both the PMOS load devices and the NMOS tail devices turned off so that it is in its ***L*** phase, and its held output data (***D02***) is fed-back to the correction pair ***Odd*** path to generate the 1st tap current pulse. This correction pulse therefore eliminats the 1st tap ISI in the input signal at the same time as the input is being amplified by the latch. Actually, when ***CKX20=1***, both the DMUX output ***D00*** and ***D01*** are available (***CKE10=1*** and ***CKO10=1)***, therefore, the ISI from post2 and post3 are cancelled by CCSA as well. Through the detailed analysis from timing diagram, the proposed 3-tap DFE works in right condition and can equalize the input data in constraint time within 1UI.

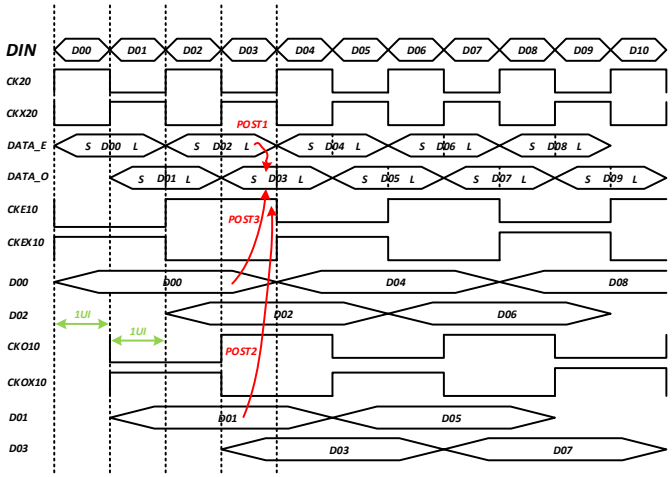
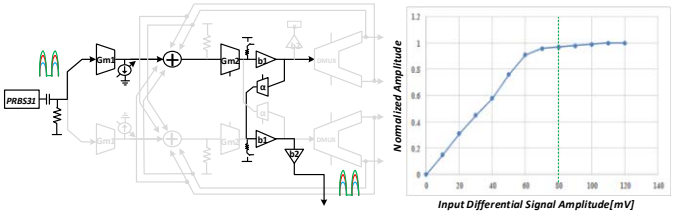


Fig.5 The timing diagram of the proposed 3-tap DFE

III. Simulation Results

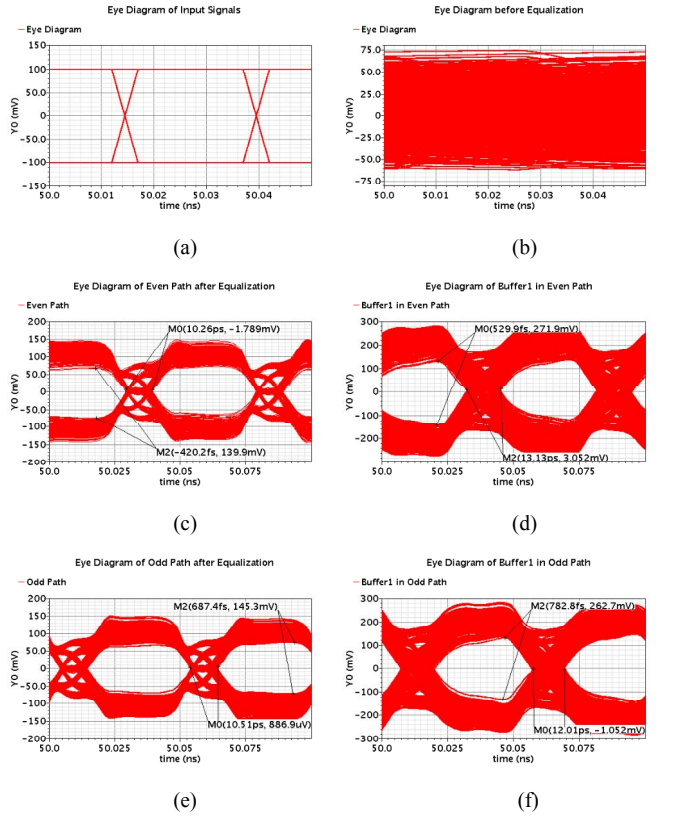
In order to testify the function of the proposed 3-tap DFE, a large number of simulation experiments are performed. First, to verify that the feedback correction can indeed be performed in a digital manner, using the circuit configuration shown in Fig.6-(a), we then characterize the input signal amplitude required to clip the feedback pair. Since the feedback pair by design has the smallest ***V**** and the largest input swing (in this configuration), its non-linearity will set the overall non-linearity of the entire chain. In other words, as we increase the input signal amplitude and measure the output amplitude, we will observe a roughly linear increase until we hit the non-linear regime of the feedback pair [2]. This measurement therefore allows us to characterize the VTC of the pair, which is shown in Fig.6-(b). As implied by the Fig.6-(b), the input cursor amplitude must at the minimum be greater than 80 mV to clip the feedback pair. It is worth noting that even if the input signal is less than 60 mV, the circuit still functions as an equalizer, albeit as a "soft-decision" equalizer (similar to [7]). Second, to detect the equalization ability, a pair of 575mm ***RLGC*** transmission lines which have a 25dB loss in 20GHz is used in the simulation. Given by the 100mV differential

PRBS-31 signals input, the eye diagram before and after DFE are shown in the Fig.7 through the cadence ADE. Both good timing and voltage margins are achieved, which demonstrates the 3-tap DFE could equalize data with serious ISI effectively.



(a) (b)

Fig.6 (a) Circuit configuration used to characterize the feedback pair's clipping voltage and (b) Simulated overall VTC



(a) (b) (c) (d) (e) (f)

Fig.7. Simulation results at SS corner, 85 °C: (a) eye diagram of input signals, (b) eye diagram after passing the RLGC channel, (c) eye diagram of even path after equalization, (d) eye diagram of buffer 1 in even path, (e) eye diagram of odd path after equalization, (f) eye diagram of buffer 1 in odd path

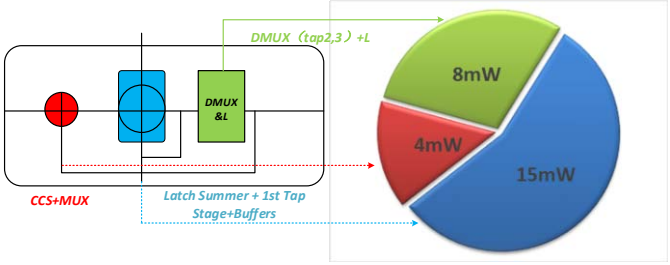


Fig.8 DFE power distribution

The total simulation power consumed by the DFE core is 27mW, as shown in Fig.8. Now that this 3-tap DFE operates at 40Gb/s, the 1st tap stage consumes about 2/3 power of the 1st tap stage in [2]. However, because the 2nd and 3rd tap stages are realized by 1 to 2 DMUXs and MUXs embed in CCSA, this slow-down data processing method and clock-control technique do great favor in saving power consumption.

Compared with other state-of-the-art designs in Table 1, our DFE achieves the high data rate at comparable or even lower energy/bit.

Table I COMPARISON TO STATE-OF-THE-ART 40+Gb/s DFE DESIGNS

Reference	[2][a]	[3][b]	**This work**[c]
Data Rate(Gb/s)	66	40	**40**
Process Technology	65nm	65nm	**65nm**
Number of DFE Taps	3	1	**3**
(Total Cancelled ISI)/Vcur	1.65	<0.63	**>1.65**
Supply(V)	1.2	1.2	**1**
Energy/bit(PJ/b)	0.7	1.13	**0.675**
Power Dissipation(mW)	46	45	**27**

[a] The channel for measurement is an on-chip mixed-signal low pass filter (LPF) with controllable coefficient values and signal amplitude.
[b] The channel loss is 15dB.
c The supply voltage is 1V for pre-simulation.

IV. CONCLUSION

This paper presented a 3-tap closed-loop DFE in 65nm CMOS technology. In order to solve the critical 1st tap closed-loop timing constraint, we proposed the combination of three optimization techniques, namely a merged latch and summer, reduced latch gain, and a dynamic latch design. Then, we suggest to merge the feedback MUX with the tap differential pairs within the CCSA to accomplish the 2nd and 3rd tap stages design. Combining these ideas enables the 3-tap power efficient DFE operate at 40Gb/s successfully.

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